Indigenous Fault Tolerant Navigation Processing Electronics for Launch Vehicle Applications

Renjis Mathew, Anwar K Backer, Deepa Sara John, Surya K M, B. Venkata Ramana, Dr. PP Mohanlal
ISRO Inertial Systems Unit, Thiruvananthapuram-695013
[1]m_renjis@vssc.gov.in

***Abstract*-This paper details the development of a novel sensor data acquisition interface & navigation processor board. The work involves a navigation processor board design, which exploits the optimum computational capability of an indigenous processor to provide a mission & vehicle independent navigation solution for a launch vehicle. This is a single board computer that acquires the inertial sensor output available in analog & pulse (digital) form, pre-processes the data, performs computations and transmits the navigation solution over 1553B communication link to the Mission Management Computer (MMC) for guidance & control. This navigation processor module named as NIPM (Navigation Interface Processor Module) has been successfully flight tested.**

I. INTRODUCTION

Sensor data acquisition and computation of navigation solution is an essential and important processing requirement for any Inertial Navigation System (INS). The generation of the navigation state vectors plays an important role in the performance of Navigation Guidance Control (NGC) system of a launch vehicle. The design of sensor data acquisition interface & navigation processing board called Navigation Interface Processor Module (NIPM), based on an indigenous processor is detailed in the paper. The embedded system design aims to overcome the timing constraints and meets the computational requirements of future missions.

II. DESIGN GOALS

A. Processor Board Hardware

The processor electronics design has been based on the following goals

i. *Indigenization:* The board is based on indigenous processor, relay drivers and DC-DC converters
ii. *Modularity and testability*: The module can be independently tested in various test beds and integrated with the sensor module to form an autonomous navigation unit
iii. *Single board design* has been achieved by use of predominantly surface mount devices
iv. *Dual Redundancy* by realization of two similar cards within a module.
v. *Noise Immunity* achieved by isolation of sensor electronics and processing electronics signals

Fig. 1 Navigation Interface Processor Module (NIPM)

The sensor data acquisition scheme consists of multichannel multiplexed analog data acquisition and multi channel digital pulse accumulators, with sufficient spare channels to cater different sensor configurations. Twenty numbers of 16-bit up/down pulse accumulators provide incremental velocity and attitude. There are 76 single-ended analog channels with input over voltage protection in ±10V range, used for health monitoring and surveillance. The data acquisition electronics and processor electronics are optically isolated. Independent DC-DC converters power these isolated sections. Sensor switch-on commands for different modes along with safety interlocks are executed from the processor board with the intervention of checkout system.

MIL-STD-1553B protocol controller is employed for communication management with MMC. NIPM is configured

as a remote terminal (RT) and uses the commands from MMC to initiate the sensor data acquisition. The overall block schematic is as below.

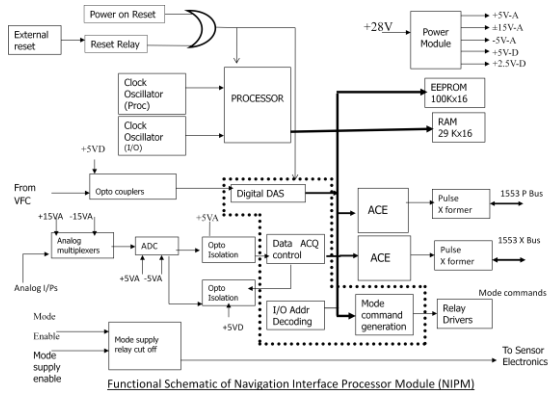

Fig. 2 Functional schematic of NIPM

Mechanical packaging is designed such that it can be stacked on top of the inertial sensor and interface electronics assembly, besides being designed for standalone tests at various test beds.

B. Firmware

The FPGA firmware implements the analog data acquisition programming interface, digital pulse counters, sensor switch-on command interface and I/O address decoding for the above functions. FPGA based implementation ensures periodic data availability to processor with minimum intervention. FPGA provides the interface to select the analog channel and to generate control signals for ADC and multiplexers. Digital pulse accumulators are implemented with simultaneous data latching of all sensor channels and sequential reading. Sensor switch-on commands are implemented as memory mapped I/Os.

C. Embedded Software

The major design criteria for the design of the embedded software are

i. *Optimal scheduling* to reduce the transport delay between data acquisition and posting of control commands
ii. *Handling of software exceptions and communication failures* to indicate the failures in the embedded system to the mission computer
iii. *Failure Detection and Isolation (FDI)* of sensors and electronics
iv. *Communication with ground system* for system validation and calibration
v. *Tight clock synchronization* with mission computer
vi. *Optimal cycle time utilization and bus load* through processor task scheduling and proper timing of 1553B messages

Major software modules include the Real time EXecutive (REX), Data Acquisition Software (DAS), checkout interface, all developed in assembly and Application modules (error compensation, FDI and navigation) in ADA.

Boot code software handles power on/external reset besides configuring the 1553B controller for RT operation. Processor self check is carried out as part on power on routine, while other diagnostics including memory and 1553 controller checks can be initiated by ground checkout.

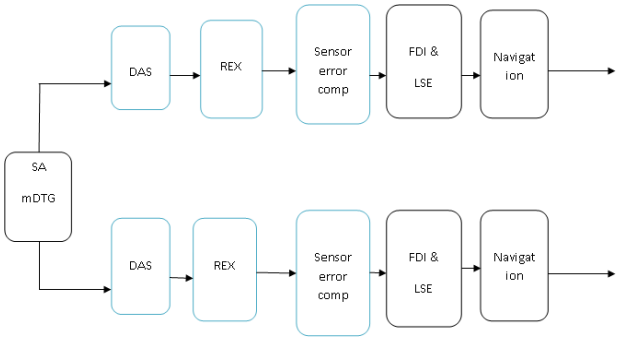

Fig. 3 Software scheme

REX, which receives its time base from an internal real time counter schedules tasks in two periodicities- a 20 ms minor cycle and 500 ms major cycle. The incremental velocity and angles from the sensor data are passed to navigation software through the REX interface. The telemetry parameters are written into the 1553 controller memory after suitable scaling and type casting. Moreover, the overall health of the unit is assessed, consolidated and passed to the mission computer for appropriate action.

There are two modes of operation for the embedded software Viz., a *flight mode* for periodic data processing and transfer and a *monitor mode* for ground surveillance and diagnostic checks.

III. FAULT TOLERANCE AND ERROR HANDLING

The INS including the module consists of six accelerometers in skewed triad hexad configuration and three gyroscopes in orthoskewed geometry. Two boards (prime & redundant) are used in hot stand-by mode. They are connected as a remote terminal to the mission computer through 1553 link in *cross strapped configuration* as shown below.

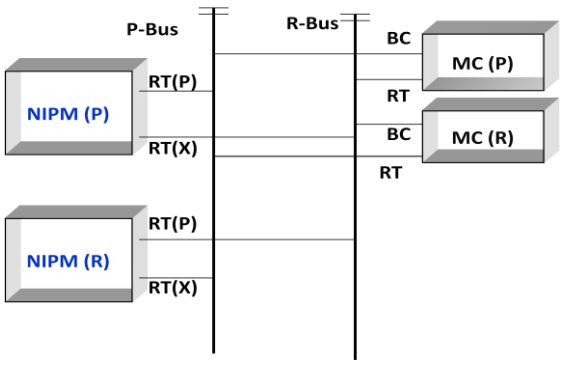

Fig. 4 Cross-strapped configuration

The system can tolerate a maximum clock drift of 150 ppm between any two clocks in the four processor NGC system shown above. Any system whose clock drifts beyond fifteen minor cycles is isolated.

Each gyro output is fed to two multiplexers to avoid any single point failure. The data acquisition scheme takes advantage of the sensor geometry to provide fail-op/fail-safe operation. Built-in hardware self check for analog and digital data acquisition ensures detection and isolation of faulty channels.

Relay cut-off for external reset circuit and sensor switch-on interface avoids spurious signals affecting *flight mode* operation.

Single bit Error Correction Double bit Error Detection (SECDED) logic handles soft errors occurring in memory. Processor ensures write protection for RAM so that critical data elements are not corrupted during operation. The program memory is also write protected by design.

Software errors like task incompletion and arithmetic errors are properly handled and indicated to the mission computer for appropriate action. Moreover, the hardware and sensor dependent parameters are loadable from checkout. This enables exhaustive testing and validation of the error handling logic and failure simulations.

IV. PERFORMANCE

NIPM has higher computational capability in comparison to the previous systems. The distributed computing system offers the following major advantages over its predecessor

i. Offers two independent navigation solutions
ii. Proper sharing of computational load offering nearly 40 % margin in both the processor units
iii. Provides an autonomous standalone navigation system for future missions
iv. The system can be easily expanded to offer integrated GPS aided navigation system
v. Reduces the transport delay between acquisition and control command by 0.5 ms
vi. Modularity of design ensures productionisation and testability of the system.

V. CONCLUSION

NIPM is a single board embedded unit which can be independently produced and tested. It exploits the computational capability of the indigenous processor and offers dual redundant navigation solution to the control and guidance system of launch vehicle. The INS employing NIPM has been successfully flight tested and offers a mission independent navigation system. The design goals viz., miniaturization, indigenization, integration of data acquisition and navigation computation in a single processor have been achieved.